REMARKS

In the Drawings

The drawings, as filed with the application, were "objected to by the Examiner," as indicated on the PTO-326 Office Action Summary. As the objections, as indicated in Paper 4, are essentially of a formatting nature, the Applicant has formalized the drawings and is submitting same to the Official Draftsman. A courtesy copy of the formalized drawings is submitted herewith for the examiner's consideration.

Rejection Under 35 U.S.C. § 102

Claims 1-4, 8, 14-17, and 21-22 were rejected 35 U.S.C. §102(b), as being anticipated by *Takasugi* (U. S. Patent No. 5,418,739). Applicants respectfully traverse this rejection.

Takasugi discloses a memory device having DRAM memory cells that are selectively connected to voltage lines. The DRAM cells then function as a ROM cell while still having the architecture of a DRAM cell. This neither teaches nor suggests Applicants' invention of a memory device that has both dynamic memory cells and ROM cells that are hard programmed to a first state.

Each DRAM memory cell (31_{ki}) of *Takasugi*, as seen in Figure 1, comprises a transistor (31_b) and a capacitor (31_a). The transistor (31_b) acts as a transfer gate and the capacitor (31_a) for data storage (see column 6, lines 11 – 18). Power and ground lines are selectively connected to the nodes between the capacitor and the transfer gate in the DRAM memory cells (31_{ki}) serving as ROM cells (see column 6, lines 21 – 28). This architecture permits writing to the ROM cells since they comprise a capacitor for data storage (see column 7, lines 15 – 29).

Applicants' invention is to a memory device that has read only memory cells that are hard programmed to a state as well as dynamic memory cells. Figures 2A and 2B clearly differentiate between the dynamic memory cells and the read only memory cells in that the transistors of the read only memory cells are connected to either a supply voltage or ground, depending on the state to which the memory cell is hard programmed, and not a capacitor for data storage. There is no provision made for writing to the ROM cells since there is a short to the supply voltage/ground or a leakage path. This is made clear by the claim elements to "a read only memory (ROM) cell hard programmed..." and the specification at paragraphs 25 and 26. Claims 14 and 17 have been amended to highlight this aspect.

Rejection Under 35 U.S.C. § 103

Claims 5-7 and 18-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Takasugi* in view of *Holland* (U.S. Patent No. 5,995,409) or *Jung et al.* (U.S. Patent No. 6,327,174).

Holland and *Jung et al.* disclose methods for permanently programming selected cells of dynamic random access memory cell arrays by shorting capacitor plates or creating dielectric breakdown so that leakage occurs. Neither *Holland* nor *Jung et al.* teach or suggest Applicants' invention as now claimed. Therefore the combination of *Takasugi* with *Holland* or *Jung et al.* cannot teach Applicants' invention.

Allowable Subject Matter

The Examiner stated that claims 9-13 are allowed.

Conclusion

In view of the above, Applicants respectfully submit that the claims are in condition for allowance and request reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicant's representatives at direct dial (612) 312-2211 if there are any questions regarding this response or if prosecution of this application may be assisted thereby. No new matter has been added and no additional fee is required by this amendment.

Respectfully submitted,

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Kenneth W. Bolvin
Reg. No. 34,125

Attorneys for Applicant
Leffert Jay & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009
telephone: (612) 312-2200
facsimile: (612) 312-2250

MARKED-UP VERSIONS OF AMENDMENTS

IN THE SPECIFICATION

[0024] Numerous methods are available to program the ROM cells. For example, U.S. Patent No. 6,134,137 issued October 17, 2000 entitled "ROM-EMBEDDED-DRAM" describes ROM cells that are fabricated to short the memory cell to either its wordline ~~of~~ or an adjacent wordline. Shorting the memory cell to its wordline results in reading a logic one (Vcc). Shorting the memory cell to an adjacent wordline results in reading a logic zero (Vss). Shorting a cell to its own wordline, however, may result in a digit line to wordline short during fabrication. As such, hard programming logic zeros may only be possible for some fabrication layouts. The hard programming technique of U.S. Patent No. 6,134,137 is an example of a technique for programming ROM cells using a DRAM fabrication. Other techniques for programming a ROM cell using a DRAM fabrication can be used without departing from the present invention. For example, ROM cells can be hard programmed by eliminating cell dielectric so that the cell plates are shorted to a program voltage, an electrical plug can be fabricated between the cell plates and shorted to a program voltage, the ROM cell can be programmed using an anti-fuse programming technique, the ROM cells can also be programmed by providing a high leakage path (not full short) such as through an active area to the substrate.

IN THE CLAIMS

14. (amended) A half-density read only memory (ROM) comprising:

an array of ROM cells each comprising first and second memory cells, the first memory cell is hard programmed in a non-volatile manner to a first voltage and the second memory cell is a volatile memory cell capacitor; and

access circuitry coupled to read each ROM cell, wherein the access circuitry electrically couples the first and second memory cells to differential sensing circuitry.

17. (amended) A method of operating a read-only memory comprising:

programming a first memory cell in a non-volatile manner to a first data state by hard programming the first memory cell to a first voltage level;

providing an un-programmed volatile memory cell; and

accessing both the first and second memory cell capacitors in response to word line signals.

21. (amended) The method of claim 17 wherein the first memory cell comprises a plate electrically coupled to ~~a bias~~ the first voltage level.

22. (amended) The method of claim 21 wherein the plate is electrically coupled to ~~a bias~~ the first voltage level that is equal to Vcc or Vss.